In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 to 12. (Canceled)

13. (Previously Presented) A digital system having a microprocessor operable to execute a rounding dot product instruction, wherein the microprocessor comprises:

storage circuitry for holding pairs of elements;

a multiply circuit connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the dot product instruction, the multiply circuit comprising a plurality of multipliers equal to the first number of pairs of elements;

an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input to a predetermined bit for mid-position rounding responsive to the rounding dot product instruction; and

a shifter connected to receive an output of the adder/subtractor circuit, the shifter operable to shift a selected amount in response to the rounding dot product instructions.

Claims 14 to 24. (Canceled)

25. (Previously Presented) A data processing apparatus comprising:

a first multiply circuit having first and second inputs and an output, said first multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a first product at said output;

a second multiply circuit having first and second inputs and an output, said second multiply circuit operable in response to a dot product instruction to multiply data received at said first and second inputs and generate a second product at said output;

an adder/subtractor circuit having first and second inputs, a mid-position carry input to a predetermined bit and an output, said first input receiving said first product from said first multiply circuit, said second input receiving said second product from said second multiply circuits, said adder/subtractor circuit operable in response to said dot product instruction to arithmetically combine said first and second products and a "1" input at said mid-position carry input of said predetermined bit thereby forming a mid-position rounded sum; and

a shifter connected to receive said mid-position rounded sum of the adder/subtractor circuit, the shifter operable to shift said mid-position rounded sum a predetermined amount in response to said dot product instruction.

26. (Previously Presented) The data processing apparatus of claim 25, wherein:

said arithmetic combination of said first and second products is an arithmetic sum.

27. (Previously Presented) The data processing apparatus of claim 25, wherein:

said dot product instruction is a dot product with negate instruction; and

said arithmetic combination of said first and second products is a difference of said second product from said first product in response to said dot product with negate instruction.

28. (Currently Amended) The data processing apparatus of

claim 25, further comprising:

a first Q shifter having an input receiving said first product from said first multiply circuit and an output supplying said first input to said adder/subtractor circuit, said first Q shifter shifting said first product an instruction specified number of bits responsive to the rounding dot product instruction; and

a second Q shifter having an input receiving said second product from said second multiply circuit and an output supplying said second input to said adder/subtractor circuit, said second Q shifter shifting said second product said instruction specified number of bits responsive to the rounding dot product instruction.

29. (Previously Presented) The data processing apparatus of claim 25, wherein:

said first multiply generates said first product in a redundant sign/magnitude format;

said second multiply circuit generates said second product in said redundant sign/magnitude format;

said adder/subtractor circuit arithmetically combines said first and second products and said "1" input at said mid-position carry input forming said mid-position rounded sum in said redundant sign/magnitude format;

a shifter shifts said mid-position rounded sum in said redundant sign/magnitude format; and

said data processing apparatus further comprises a carry save adder to 2's complement converter having an input receiving said shifted mid-position rounded sum in said redundant sign/magnitude format and an output generating a corresponding normal coded format.